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HALOGEN GETTERING METHOD FOR FORMING FIELD EFFECT TRANSISTOR (FET) DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates generally to methods for forming field effect transistor (FET) devices. More particularly, the present invention relates to methods for forming field effect transistor (FET) devices with enhanced performance.

2. Description of the Related Art

[0002] Common in the semiconductor product fabrication art is the fabrication and use of field effect transistor devices as switching devices within logic semiconductor products, memory semiconductor products and embedded logic and memory semiconductor products.

[0003] While field effect transistor devices are thus common in the semiconductor product fabrication art and often essential for fabricating semiconductor products, field effect transistor devices are nonetheless not entirely without problems.

[0004] In that regard, as semiconductor product integration levels have increased and semiconductor device dimensions have decreased, it has become increasingly difficult to form within semiconductor products field effect transistor devices with enhanced performance.

[0005] It is thus desirable in the semiconductor product fabrication art to fabricate field effect transistor devices with enhanced performance.

[0006] It is towards the foregoing object that the present invention is directed.

[0007] Various methods have been disclosed within the semiconductor product fabrication art for forming field effect transistor devices with desirable properties.

[0008] Included but not limiting among the methods are those disclosed within: (1) Yeh et al., in U.S. Patent No. 5,393,686 (a halogen gettering method for forming within a field effect transistor device a gate dielectric layer such as to form the field effect transistor device with enhanced performance); and (2) Grider et al., in U.S. Patent No. 6,093,659 (a halogen doping method for forming within a semiconductor substrate a pair of gate dielectric layers with differing thicknesses such as to provide a pair of field effect transistor devices with differing performance properties).

[0009] Desirable in the semiconductor product fabrication art are additional methods for forming field effect transistor devices with enhanced performance.

[0010] It is towards the foregoing object that the present invention is directed.

SUMMARY OF THE INVENTION

[0011] A first object of the invention is to provide a method for forming a field effect transistor device.

[0012] A second object of the invention is to provide a method in accord with the first object of the invention, wherein the field effect transistor device is formed with enhanced performance.

[0013] In accord with the objects of the invention, the invention provides a method for forming a gate dielectric layer for use within a field effect transistor device.

[0014] To practice the method of the invention, there is first provided a semiconductor substrate. The semiconductor substrate is then thermally oxidized within a thermal oxidizing atmosphere comprising a halogen getter material to form a gate dielectric layer upon a thermally oxidized semiconductor substrate.

[0015] The invention provides a method for forming a field effect transistor device, where the field effect transistor device is formed with enhanced performance.

[0016] The invention realizes the foregoing object by employing a thermal oxidizing atmosphere comprising a halogen getter material when thermally oxidizing a semiconductor substrate such as to form a gate dielectric layer upon a thermally oxidized semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The objects, features and advantages of the invention are understood within the context of the Description of the Preferred Embodiment, as set forth below. The Description of the Preferred Embodiment is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

[0018] Fig. 1, Fig. 2, Fig. 3, Fig. 4 and Fig. 5 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages of forming a pair of field effect transistor devices within a semiconductor product in accord with a preferred embodiment of the invention.

[0019] Fig. 6 shows a graph of Negative Bias Temperature Instability (NBTI) Lifetime versus Thermal Oxidizing Atmosphere Composition (with and without presence of chlorine getter material) for forming a pair of field effect transistor devices in accord with the invention and not in accord with the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0020] The invention provides a method for forming a field effect transistor device, where the field effect transistor device is formed with enhanced performance.

[0021] The invention realizes the foregoing object by employing a thermal oxidizing atmosphere comprising a halogen getter material when thermally oxidizing a semiconductor

substrate such as to form a gate dielectric layer upon a thermally oxidized semiconductor substrate.

[0022] Fig. 1 to Fig. 5 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages of fabricating a pair of field effect transistor devices in accord with a preferred embodiment of the invention.

[0023] Fig. 1 shows a schematic cross-sectional diagram of the semiconductor product at an early stage in its fabrication in accord with the preferred embodiment of the invention.

[0024] Fig. 1 shows a semiconductor substrate 10 having formed therein a series of isolation regions 12a, 12b and 12c which define a pair of active regions 11a and 11b of the semiconductor substrate 10.

[0025] Within the invention, the semiconductor substrate 10 is formed of a thermally oxidizable semiconductor material, such as but not limited to a thermally oxidizable silicon semiconductor material or a thermally oxidizable silicon-germanium alloy semiconductor material. More typically, the semiconductor substrate 10 is formed of a thermally oxidizable silicon semiconductor material which may have formed therein doped regions as are appropriate for forming the pair of field effect transistor devices within the semiconductor product whose schematic cross-sectional diagram is illustrated in Fig. 1.

[0026] Within the invention, the series of isolation regions 12a, 12b and 12c may be formed employing methods and materials as are otherwise generally conventional in the semiconductor product fabrication art, to provide isolation regions such as but not limited to local oxidation of silicon oxidation regions and shallow trench isolation regions.

[0027] Within the invention, the semiconductor product as illustrated in Fig. 1 will typically and preferably be cleaned within an aqueous cleaning solution such as an ammonia and hydrogen peroxide aqueous cleaning solution.

[0028] Fig. 2 shows a schematic cross-sectional diagram illustrating the results of further processing of the semiconductor product of Fig. 1.

[0029] Fig. 2 shows the results of thermally oxidizing the semiconductor substrate 10 as illustrated in Fig. 1 within a first thermal oxidizing atmosphere 13 to form a pair of first gate dielectric layers 14a and 14b upon the pair of active regions 11a and 11b of a once thermally oxidized semiconductor substrate 10'.

[0030] Within the invention, the first thermal oxidizing atmosphere 13 comprises a halogen getter material when forming the pair of first gate dielectric layers 14a and 14b upon the pair of active regions 11a and 11b of the once thermally oxidized semiconductor substrate 10'. The halogen getter material may comprise a fluorine, chlorine, iodine or bromine

halogen getter material, but preferably a chlorine halogen getter material. Preferable chlorine halogen getter materials include, but are not limited to, molecular chlorine (i.e., Cl_2), hydrogen chloride (i.e., HCl) and one to three carbon atom perchlorocarbons and hydrochlorocarbons. Within the invention, 1,2-trans-dichloroethylene ($C_2H_2Cl_2$) is a particularly preferred chlorine halogen getter material.

[0031] The first thermal oxidizing atmosphere 13 may be a dry thermal oxidizing atmosphere (i.e., absent moisture) or a wet thermal oxidizing atmosphere (i.e., containing moisture). The first thermal oxidizing atmosphere 13 may be a purely oxidizing atmosphere (i.e., typically consisting of oxygen) or a nitriding and oxidizing atmosphere (i.e., typically consisting of a nitrogen containing nitridant and an oxygen containing oxidant, such as nitrous oxide or nitric oxide).

[0032] Typically, the first thermal oxidizing atmosphere 13 also employs: (1) a reactor chamber pressure of from about 700 to about 800 torr; (2) a temperature of from about 750 to about 850 degrees centigrade; (3) an oxidant material (typically oxygen) flow rate of from about 3000 to about 5000 standard cubic centimeters per minute (sccm); (4) a halogen getter material flow rate of from about 200 to about 300 standard cubic centimeters per minute (sccm); and (5) a thermal oxidation process time of from about 15 to about 35 minutes. Typically each of the pair of first gate dielectric layers 14a and 14b is formed to a thickness of from about 50 to about 60 angstroms.

[0033] Fig. 3 shows a schematic cross-sectional diagram illustrating the results of further processing of the semiconductor product of Fig. 2.

[0034] Fig. 3 shows the results of stripping the first gate dielectric layer 14b from the active region 11b of the once thermally oxidized semiconductor substrate 10' as illustrated within the schematic cross-sectional diagram of Fig. 2.

[0035] Within the invention, the first gate dielectric layer 14b may be stripped from the semiconductor product as illustrated in Fig. 2 to provide the semiconductor product as illustrated in Fig. 3 while employing masked stripping methods as are conventional in the semiconductor product fabrication art. Such masked stripping methods will typically employ a masking of the first gate dielectric layer 14a with a mask layer, such as a photoresist mask layer, and a stripping of the first gate dielectric layer 14b with a hydrofluoric acid containing etchant under circumstances where the first gate dielectric layer 14b is formed of a non-nitrided silicon oxide material.

[0036] Fig. 4 shows a schematic cross-sectional diagram illustrating the results of further processing of the semiconductor product of Fig. 3.

[0037] Fig. 4 shows the results of forming: (1) a second gate dielectric layer 16a upon the first gate dielectric layer 14a; and (2) forming a second gate dielectric layer 16b upon the

active region 11b of a twice thermally oxidized semiconductor substrate 10'' incident to thermal oxidation within a second thermal oxidizing atmosphere 15.

[0038] Within the invention, the second thermal oxidizing atmosphere 15 is otherwise generally analogous to the first thermal oxidizing atmosphere 13, but the second thermal oxidizing atmosphere 15 is preferably a nitriding thermal oxidizing atmosphere which employs a nitriding oxidant such as nitrous oxide or nitric oxide and the second thermal oxidizing atmosphere 15 does not necessarily (and generally does not) comprise a halogen getter material. Thus, each of the pair of second gate dielectric layers 16a and 16b is preferably formed of a nitrided silicon oxide material, rather than a non-nitrided silicon oxide material from which is preferably formed each of the pair of first gate dielectric layers 14a and 14b. Typically, each of the second gate dielectric layers 16a and 16b is formed to a thickness of from about 10 to about 25 angstroms.

[0039] Fig. 5 shows a schematic cross-sectional diagram illustrating the results of further processing of the semiconductor product of Fig. 4.

[0040] Fig. 5 shows the results of: (1) forming upon the second gate dielectric layer 16a a gate electrode 18a and forming into the active region 11a of the twice thermally oxidized semiconductor substrate 10'' a pair of source/drain regions 20a and 20b to form a first field effect transistor device within and upon the active region 11a of the twice thermally oxidized semiconductor substrate 10''; and (2) forming

upon the second gate dielectric layer 16b a gate electrode 18b and forming into the active region 11b of the twice thermally oxidized semiconductor substrate 10'' a pair of source/drain regions 20c and 20d to form a second field effect transistor device within and upon the active region 11b of the twice thermally oxidized semiconductor substrate 10''.

[0041] Within the invention, the pair of gate electrodes 18a and 18b may be formed employing methods and materials as are generally conventional in the semiconductor product fabrication art. Typically, the pair of gate electrodes 18a and 18b is formed of a doped polysilicon (having a dopant concentration of from about 1E20 to about 1E22 dopant atoms per cubic centimeter) or polycide (doped polysilicon/metal silicide stack) material, formed to a thickness of from about 1500 to about 3500 angstroms. In addition, the series of source/drain regions 20a, 20b, 20c and 20d may also be formed employing methods as are generally conventional in the semiconductor product fabrication art, to form the series of source/drain regions 20a, 20b, 20c and 20d of a dopant concentration from about 1E18 to about 1E20 dopant atoms per cubic centimeter, and of an appropriate dopant polarity.

[0042] The semiconductor product as illustrated in Fig. 5 provides a semiconductor product fabricated in accord with the preferred embodiment of the invention. The semiconductor product has formed therein a pair of field effect transistor devices, one having a laminated bilayer nitrided silicon oxide/non-nitrided silicon oxide gate dielectric layer, the

other having a single layer nitrided silicon oxide gate dielectric layer. Within the invention, the first field effect transistor device having the bilayer laminated gate dielectric layer is generally employed for semiconductor product power or input/output functions, where protection from transient voltages swings may be of concern. The second field effect transistor device having the thinner single layer gate dielectric layer is typically employed within logic applications where transistor speed is an important consideration.

[0043] Within each of the first field effect transistor device and the second field effect transistor device, a gate dielectric layer is formed with enhanced performance insofar as the gate dielectric layer is formed employing a thermal oxidation method that employs a thermal oxidizing atmosphere comprising a halogen getter material when forming the gate dielectric layer. The invention thus differs from related methods that may employ either: (1) a halogen dopant treatment of a semiconductor substrate prior to forming a gate dielectric layer thereupon; or (2) a halogen gettering treatment of a gate dielectric layer after it is formed. Alternatively stated, the invention employs a halogen getter treatment in-situ when forming a gate dielectric layer upon a semiconductor substrate.

Example

[0044] To illustrate the value of the invention, a semiconductor product having formed therein two field effect transistor devices was fabricated in accord with the preferred embodiment of the invention.

[0045] The semiconductor product comprised a semiconductor substrate having formed thereupon a pair of non-nitrided silicon oxide gate dielectric layers formed employing a first thermal oxidation of a semiconductor substrate within a first thermal oxidizing atmosphere comprising a transdichloroethylene chlorine getter material when thermally oxidizing the semiconductor substrate. The first thermal oxidation method also employed: (1) a reactor chamber pressure of about 760 torr; (2) a thermal oxidation temperature of about 800 degrees centigrade; (3) a dry oxygen oxidant at a flow rate of about 4000 standard cubic centimeters per minute; and (4) a transdichloroethylene flow rate of about 250 standard cubic centimeters per minute. The first thermal oxidation method provided a pair of first gate dielectric layers upon a pair of active regions of the semiconductor substrate, each gate dielectric layer having a thickness of about 50 angstroms.

[0046] One of the silicon oxide gate dielectric layers was then stripped from one of the active regions of the semiconductor substrate, while employing an aqueous hydrofluoric acid etchant at elevated temperature.

[0047] A pair of second gate dielectric layers was then formed, one each upon: (1) the remaining non-nitrided silicon oxide gate dielectric layer; and (2) the remaining uncovered active region of the semiconductor substrate. This second pair of gate dielectric layers was formed of a nitrided silicon oxide material formed employing a thermal oxidation method which employed a dry nitrous oxide oxidant, rather than a dry oxygen

oxidant, and with no transdichloroethylene chlorine getter material or any other getter material.

[0048] A pair of field effect transistor devices was then fabricated within the pair of active regions of the semiconductor substrate while employing gate patterning and source/drain region ion implantation as is otherwise generally conventional in the semiconductor product fabrication art. For comparison purposes, an additional pair of field effect transistor devices was fabricated in accord with the foregoing process description, but without a halogen or chlorine getter material within either the first thermal oxidizing method or the second thermal oxidizing method.

[0049] Negative bias temperature instability lifetime measurements were then obtained for each of the two series of field effect transistor devices. Results of the measurements are shown within the graph of Fig. 6, which illustrates negative bias temperature instability lifetimes as a function of silicon oxide gate oxidation process (either with transdichloroethylene chlorine getter material or without transdichloroethylene chlorine getter material within the first thermal oxidizing atmosphere). Within Fig. 6, square data points correspond with the bilayer (non-nitrided silicon oxide/nitrided silicon oxide) gate dielectric layers of aggregate thickness about 65 angstroms while diamond shaped data points correspond with the single layer (non-nitrided silicon oxide) gate dielectric layers of thickness about 20 angstroms. As is illustrated within Fig. 6, for field effect transistor devices having formed therein either

the single layer gate dielectric layers or the bilayer gate dielectric layers, significant increases in negative bias temperature instability lifetimes are observed when employing a thermal oxidation method employing a halogen gettering material for forming a first gate dielectric layer formed of a non-nitrided silicon oxide material, whether or not the first gate dielectric layer is stripped prior to forming a nitrided silicon oxide gate dielectric layer.

[0050] As is understood by a person skilled in the art, the preferred embodiment and example of the invention are illustrative of the invention rather than limiting of the invention. Revisions and modifications may be made to methods, materials, structures and dimensions in accord with the preferred embodiment and example of the invention, while still providing a semiconductor product in accord with the invention, further in accord with the accompanying claims.